R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The Applicants thank Examiner Wilson for the indication of allowable matter in claims 6-8 and 15-18.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in claims 5 and 12. The perceived allowable matter of claim 6 has been adjusted to depend from claim 1, instead of claim 5. Thus, no new matter has been added and no new issues are believed to be raised.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-5, 9-14, 19 and 20 under 35 U.S.C. §102(e) as being anticipated by Edwards et al., U.S. Publication No. 2003/0056154 (hereafter Edwards) is respectfully traversed in part and should be withdrawn.

Edwards concerns a system and method for communicating with an integrated circuit (Title).

In contrast, claim 1 provides a connector circuit configured to couple a trace circuit to a selected processor of a plurality of processors in response to a select signal. Despite the assertion in the Office Action, the communication link 104 of Edwards (asserted similar to the claimed connector circuit) does not appear to couple **in response to a select signal.** Therefore,

Edwards does not appear to disclose or suggest a connector circuit configured to couple a trace circuit to a selected processor of a plurality of processors in response to a select signal as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly and concisely (a) identify a signal in Edwards allegedly similar to the claimed select signal and (b) show where Edwards discloses the communication link 104 coupling in response to the alleged signal or (ii) withdraw the rejection.

Claim 1 further provides a boundary scan chain connected to each of a plurality of processors and a trace circuit. Despite the assertion in the Office Action, Edwards appears to be silent regarding a JTAG chain connected to a processor 102 (asserted similar to one of the claimed processors). Therefore, Edwards does not appear to disclose or suggest a boundary scan chain connected to each of a plurality of processors and a trace circuit as presently claimed. Claims 9 and 19 provide language similar to claim 1. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Edwards allegedly discusses the JTAG chain connected to the processors or (ii) withdraw the rejection.

Claim 3 provides that the connector circuit is further configured to transfer a first test data stream received by a selected processor through a boundary scan chain to a trace circuit. Despite the assertion in the Office Action, Edwards appears to be silent regarding the communication link 104 (asserted similar to the claimed connector circuit) transferring test data

streams through the JTAG chain (asserted similar to the claimed boundary scan chain). Therefore, Edwards does not appear to disclose or suggest a connector circuit configured to transfer a first test data stream received by a selected processor through a boundary scan chain to a trace circuit as presently claimed. As such, the Examiner is respectfully requested to either (i) explain how the cited text and figures of Edwards allegedly anticipates the claim limitations or (ii) withdraw the rejection.

Claim 4 provides that the connector circuit is further configured to transfer a second test data stream from a trace circuit through a boundary scan chain to a selected processor. Despite the assertion in the Office Action, Edwards appears to be silent regarding the communication link 104 (asserted similar to the claimed connector circuit) transferring test data streams through the JTAG chain (asserted similar to the claimed boundary scan chain). Therefore, Edwards does not appear to disclose or suggest a connector circuit configured to transfer a second test data stream from a trace circuit through a boundary scan chain to a selected processor as presently claimed. As such, the Examiner is respectfully requested to either (i) explain how the cited text and figures of Edwards allegedly anticipates the claim limitations or (ii) withdraw the rejection.

Claim 5 provides that the connector circuit comprises a first circuit and a second circuit. Despite the assertion in the Office Action, Edwards appears to be silent regarding the communication link 104 (asserted similar to the claimed connector

circuit) comprises a first circuit and a second circuit as presently claimed. As such, the Examiner is respectfully requested to either (i) identify the elements of the communication link 104 that allegedly anticipate the claimed first circuit and the second circuit or (ii) withdraw the rejection.

Claim 5 further provides that the connector circuit presents a predetermined logic state and a second predetermined logic state to the processors other than a selected processor. In contrast, Edwards appears to be silent regarding the communication link 104 (asserted similar to the claimed connector circuit) presenting predetermined logic states to processors other than the processor 102 (asserted similar to the claimed selected processor). Therefore, Edwards does not appear to disclose or suggest presenting a predetermined logic state and a second predetermined logic state to the processors other than a selected processor as presently claimed. Claims 13 and 14 provides predetermined logic states similar to claim 5. As such, the Examiner is respectfully requested to either (i)(a) clearly identify the processors other than the processor 102 in Edwards allegedly connected to the communication link 104 and (b) show where Edwards discloses presenting predetermined logic states to the other processors as claimed or (ii) withdraw the rejections for claims 5, 13 and 14.

Claim 12 provides a step for transferring a second test data stream from a trace circuit to a selected processor. Despite the assertion in the Office Action, Edwards appears to be silent regarding transferring test data streams from a debug circuit 103

(asserted similar to the claimed trace circuit) and the processor 102 (asserted similar to the claimed selected processor). In particular, the only cited text of Edwards that discusses transfers from the debug circuit 103 to the processor 102 is paragraph 0058 which states that the communication link 104 transfers "state and processor control information from the debug circuit 103 to the processor 102." The rest of Edwards appears to be silent regarding the communication link 104 transferring **test data streams** to the processor 102. Therefore, Edwards does not appear to disclose or suggest a step for transferring a second test data stream from a trace circuit to a selected processor as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify where Edwards discusses test data streams on the communication link 104 from the debug circuit 103 to the processor 102 or (ii) withdraw the rejection.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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